Work Plan – Final Project

Jessica Diller

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| Task | Time Estimate | Date Finished Estimate | Time Actual | Date Finished Actual |
| Basic Understanding  Successive Approx.  Flash  ~~Pipeline~~  **Comparison**  Think about how to quantify and qualify characteristics for comparison  Find & clarify comparison data  Successive Approx.  Flash  ~~Pipeline~~  **Verilog implementation**  Black box diagrams-inputs/outputs  Successive Approximation  Flash  ~~Pipeline~~  Successive Approximation  S.A. Register  DAC  Sample and Hold Circuit  Comparator  ~~x10?~~  Integration  Mux  Shift Register  Test documentation  ~~Flash~~  ~~Analog Ref~~  ~~PreAmp~~  ~~Comparator~~  ~~Decoder (Errors)~~  ~~De-Multiplexer~~  ~~x8?~~  Write Up  Write up what I did  Write up why I did  Write up Verilog method  Poster and Presentation Prep | 1 hour  1 hour  ~~1 hour~~  2 hours  2 hours  2 hours  ~~2 hours~~  15 min  15 min  ~~15 min~~  1 hour  1 hour  1 hour  1 hour  ~~1 hour~~  NEW  NEW  NEW  NEW  ~~15 min~~  ~~1 hour~~  ~~-done-~~  ~~1 hour~~  ~~1 hour~~  ~~3 hours~~  NEW  NEW  NEW  NEW | December 7th  December 7th  ~~December 7~~~~th~~  December 7th  December 7th  December 10th  ~~stretch~~  December 7th  December 10th  ~~December 10~~~~th~~  December 10th  December 10th  December 10th  December 10th  ~~December 14~~~~th~~  NEW  NEW  NEW  NEW  NEW  NEW  NEW  NEW | 1 hour  1 hour  ???  ???  ???  2 hours  1 hour  2 hour  3 hours  30 min  30 min  3 hours  30 min  30 min  3 hours  1 hour  1 hour  1 hour | December 7  December 7  ???  ???  ???  December 7  December 11  December 12  December 12  December 13  December 13  December 14  December 14  December 14  December 15  December 15  December 15  December 15  December 15 |